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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/727,257	12/02/2003	Gary Shipton	PEATIUS	6710	
24011	7590 09/19/2006		EXAMINER		
SILVERBRO 393 DARLIN	OOK RESEARCH PT	Y LTD	WEINMAN, SEAN M		
BALMAIN,	NSW 2041		ART UNIT	PAPER NUMBER	
AUSTRALIA	•	•	2115		
			DATE MAILED: 09/19/2006		

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)				
	10/727,257	SHIPTON ET AL.				
Office Action Summary	Examiner	Art Unit				
	Sean Weinman	2115				
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the c	orrespondence ad	dress –			
A SHORTENED STATUTORY PERIOD FOR REPLY WHICHEVER IS LONGER, FROM THE MAILING DA. - Extensions of time may be available under the provisions of 37 CFR 1.1: after SIX (6) MONTHS from the mailing date of this communication. - If NO period for reply is specified above, the maximum statutory period value and the reply within the set or extended period for reply will, by statute any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	ATE OF THIS COMMUNICATION 36(a). In no event, however, may a reply be timution and will expire SIX (6) MONTHS from a cause the application to become ABANDONE	N. nely filed the mailing date of this co D (35 U.S.C. § 133).				
Status						
1)⊠ Responsive to communication(s) filed on <u>amer</u>	ndment filed on July 3, 2006.					
·	action is non-final.					
•						
closed in accordance with the practice under E	Ex parte Quayle, 1935 C.D. 11, 45	53 O.G. 213.				
Disposition of Claims						
4) Claim(s) <u>1-5</u> is/are pending in the application.						
4a) Of the above claim(s) is/are withdrawn from consideration.						
5) Claim(s) is/are allowed.						
6)⊠ Claim(s) <u>1-5</u> is/are rejected.	6)⊠ Claim(s) <u>1-5</u> is/are rejected.					
	, — · · · · · · · · · · · · · · · · · ·					
8) Claim(s) are subject to restriction and/o	r election requirement.					
Application Papers						
9)☐ The specification is objected to by the Examine						
10) \boxtimes The drawing(s) filed on <u>02 December 2003</u> is/are: a) \boxtimes accepted or b) \square objected to by the Examiner.						
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).						
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).						
11)☐ The oath or declaration is objected to by the Ex	caminer. Note the attached Office	Action or form P	10-152.			
Priority under 35 U.S.C. § 119						
 12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority application from the International Burea * See the attached detailed Office action for a list 	s have been received. s have been received in Applicati rity documents have been receive u (PCT Rule 17.2(a)).	ion No ed in this National	Stage			
Attachment(s) 1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO/SB/08)	4) Interview Summary Paper No(s)/Mail D 5) Notice of Informal F	ate				
Paper No(s)/Mail Date	6)					

DETAILED ACTION

This action is responsive to the amendment filed on July 3, 2006. Claims 1-5 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Muller (US Patent No. 4,644,494) in view of Schu et al. (US Patent No. 5,973,968).

As per claim 1, Muller teaches the claimed invention comprising:

An integrated circuit (Figure 1Reference character 40) comprising a processor (Figure 3 Reference character 32 and Col. 7 lines 43-49), a memory that the processor can access (Figure 3 Reference character 38), a memory access unit for controlling accesses to the memory (Figure 3 Reference character 32), an input for receiving power for the integrated circuit from an external power source (Figure 2 Reference character 62), and a power detection unit (Figure 1 Reference character 52), the power detection unit being configured to:

monitor a quality of power supplied to the input (Col. 2 lines 29-51);

in the event the quality of the power drops below a predetermined threshold, preventing subsequent words in any multi-word write currently being performed from being written to the memory. (Col. 9 lines 49-54).

Muller, however, does not teach that in the event that the power drops below a threshold, disabling power to the circuitry used for writing to the memory so that the memory's ability to write data to the memory is disabled. Specifically, Muller teaches in the event that the power drops below a predetermined threshold disabling the write/read function of the memory to prevent error in the memory. Muller fails to teach the disabling of the power supply to the write circuitry so that the memory cannot be written to when the power drops below a threshold.

Schu et al. teach a method for protecting memory that in the event of a loss of power the power to the write logic circuit can be selectively removed so that the memory will not be written to when the memory is unreliable. Schu et al. teaches the claimed invention comprising in the event the quality of the power drops below a predetermined threshold, disabling a power supply to circuitry for use in writing to the memory, such that the memory access unit's ability to alter data in the memory is disabled prior to address or data values to be written to the memory becoming unreliable due to failing power (Col. 2 lines 56-63). In summary, Schu et al. teaches that when the power is loss the power to the write logic circuitry is removed so that the data cannot be written to unreliable memory.

It would have been obvious to one of ordinary skill in the art to combine the teachings of Muller and Schu et al. because they both teach in the event that the power drops below a predetermined threshold disabling the write function of the memory to prevent error in the memory. Schu et al. teaches disabling of the power supply to the write circuitry so that the memory cannot be written to when the power drops below a threshold.

As per Claim 2, Muller teaches the circuit, wherein the memory is EEPROM (Col.8, lines 15-16) It is known in the area of the pertaining art that flash memory is a type of EEPROM.

Also, it would have been obvious to one of ordinary skill in the art that the power supply can be one or more charge pumps since a charge pump are often the best choice for powering an application requiring a combination of low power and low cost.

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As per Claim 3, it would have been obvious to one of ordinary skill in the art that memory contents cannot be altered after the voltage output by the power supply drops so rapidly that the voltage to the memory is too low and before the address and data values become invalid.

As per Claim 4, Muller teaches the apparatus configured to cause a reset of at least some of the circuitry on the circuit following disabling of the power supply (Abstract, lines 16-19).

As per Claim 5, it would have been obvious to one of ordinary skill in the art that the said circuit designed to have a variable delay between the disabling of the power supply and causing the reset.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean Weinman whose phone number is (571) 272-2744. The examiner can normally be reached on Monday-Friday from 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (571) 272-3667. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

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Sean Weinman Examiner Art Unit 2115

CHUN CAO PRIMARY EXAMINER